TX73L64 3-Level, 64-Channel Transmitter with On-Chip Beamformer, T/R Switch, 32-Channel Multiplexed Receivers with LNA

1 Features

- Transmitter supports:
  - 64-channel 3-level pulser and active transmit/ receive (T/R) switch
- 3-level pulser:
  - Maximum output voltage: ±100V
  - Minimum output voltage: ±1V
  - Maximum output current: 1A
  - True return to zero to discharge output to ground
  - Second harmonic of –40dBc at 5MHz
  - –3-dB Bandwidth with 400Ω || 125pF load
    - 22MHz for a ±100-V supply
  - Very low receive power: 2.8mW/ch
- Active transmit/receive (T/R) switch with:
  - Turn on resistance of 22Ω
  - Turn on and Turn off time: 100ns
  - 2:1 Channel Muxing to LNA input
- LNA
  - Supports a maximum input swing of 500mVpp
  - Gain of 24dB
  - HD2 of -55 dBc and HD3 of 40dBc at 5MHz
  - Programmable input impedance to match source impedance 100, 200. 400 and 800Ω with DTGC support
- On-chip beam former with:
  - Channel based T/R switch on and off controls
  - Delay resolution: half beamformer clock period, minimum 2.5ns
  - Maximum delay: 2^{14} beamformer clock period
  - Maximum beamformer clockspeed: 200MHz
  - On-Chip RAM for pattern and delay profile
  - One 512 × 32 memory to store beam-former pattern and delay for a group of 4 channels
  - Global repeat feature present, enabling long duration patterns
- High-speed (400MHz maximum), 2-lane LVDS serial programming interface.
  - Low programming time: ≈1µs for delay profile update
  - 32-bit Checksum to detect wrong SPI writes
- Supports CMOS serial programming interface (50MHz maximum)
- High reliability features:
  - Internal temperature sensor and automatic thermal shutdown
  - No specific power sequencing requirement
  - Error flag register to detect faulty conditions
  - Integrated passives for the floating supplies and bias voltages
  - Small package: FC-BGA-196 (12mm × 12mm) with 0.8mm pitch

2 Applications

- Ultrasound imaging system
- Piezoelectric driver
- In-probe ultrasound imaging

3 Description

TX73L64 is a highly integrated, high-performance transmitter device for ultrasound imaging system. The device has total 64 pulser circuits, 64 transmit/ receive switches (referred as T/R or TR switches), 32 LNA circuits, and supports on-chip beamformer (TxBF). The T/R switches also perform a 2:1 multiplexing operation to multiplex inputs of 2 channels to 1 LNA. The device also integrates on-chip floating power supplies that reduce the number of required high voltage power supplies.

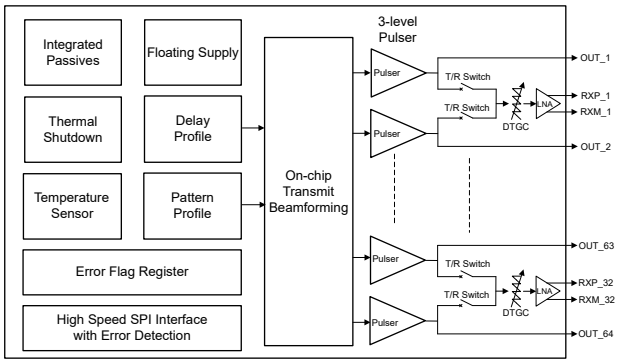
TX73L64 has a pulser circuit that generates three-level high voltage pulses (up to ±100 V) that is used to excite multiple channels of an ultrasound transducer. The device supports total 64 outputs. The maximum output current is 1A.

Device can be used as a transmitter device for many applications like ultrasound imaging, non-destructive testing, SONAR, LIDAR, marine navigation system, brain imaging systems and so on.

Package Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TX73L64	FC-BGA-196	12.0mm × 12.0mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Block Diagram

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop designs are listed below.

4.1 Documentation Support

Abbreviation	Comment
PRT	Pulse Repetition Time. Represent TR_BF_SYNC period
PRF	Pulse Repetition Frequency. Represent TR_BF_SYNC frequency
Receive Mode	Duration in which T/R switch of all the channels are in ON state
High Voltage Supplies	AVDDP_HV and AVDDM_HV are collectively referred as high voltage supplies
Low Voltage Supplies	AVDDP_5, AVDDM_5, and AVDDP_1P8 supplies are collectively referred as low voltage supplies
SPI	Serial program interface

4.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

4.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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4.4 Trademarks

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4.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

4.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
April 2025	*	Initial Release

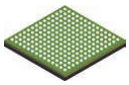
6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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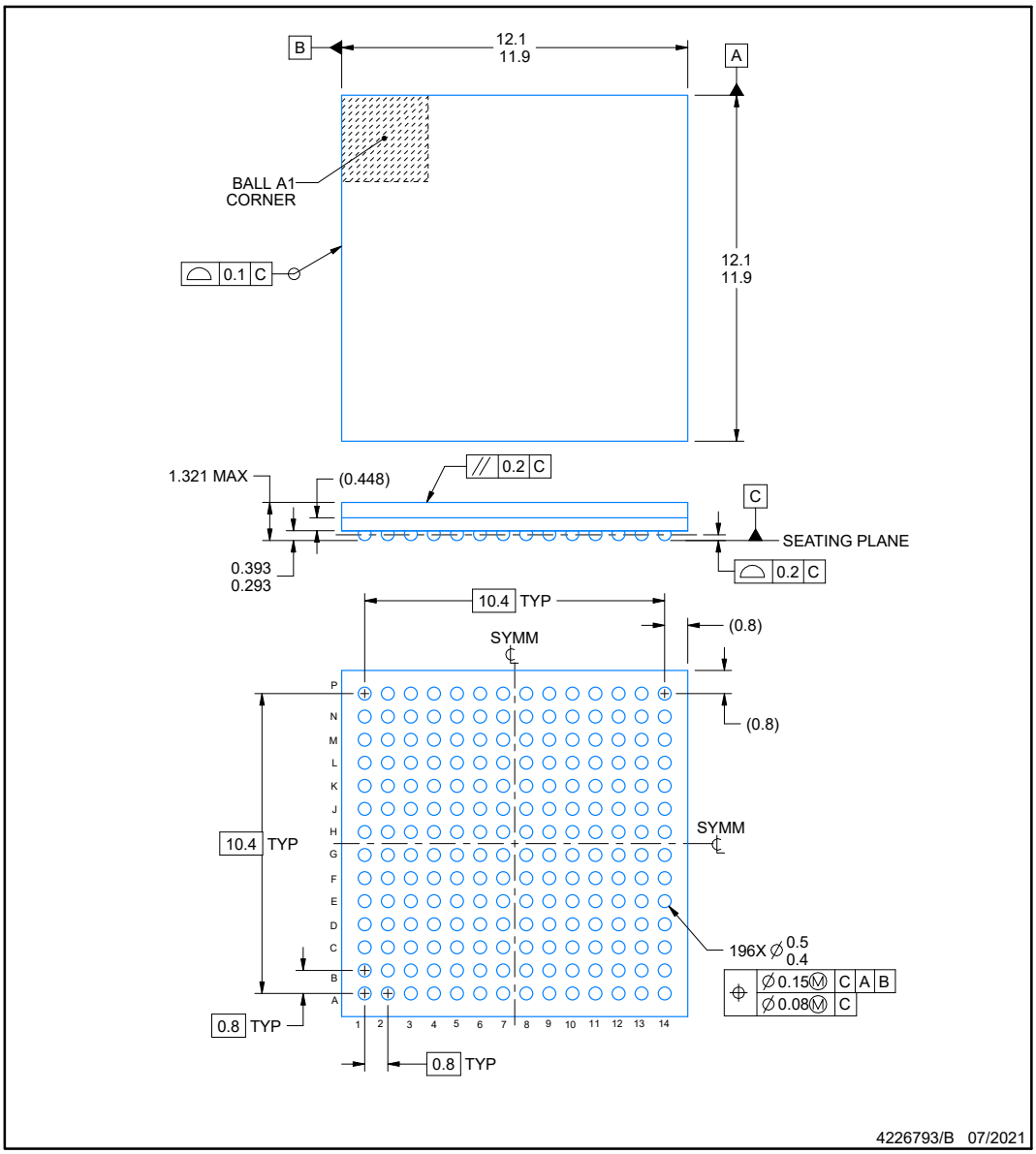
PACKAGE OUTLINE

ACP0196A



FCBGA - 1.321 mm max height

BALL GRID ARRAY



NOTES:

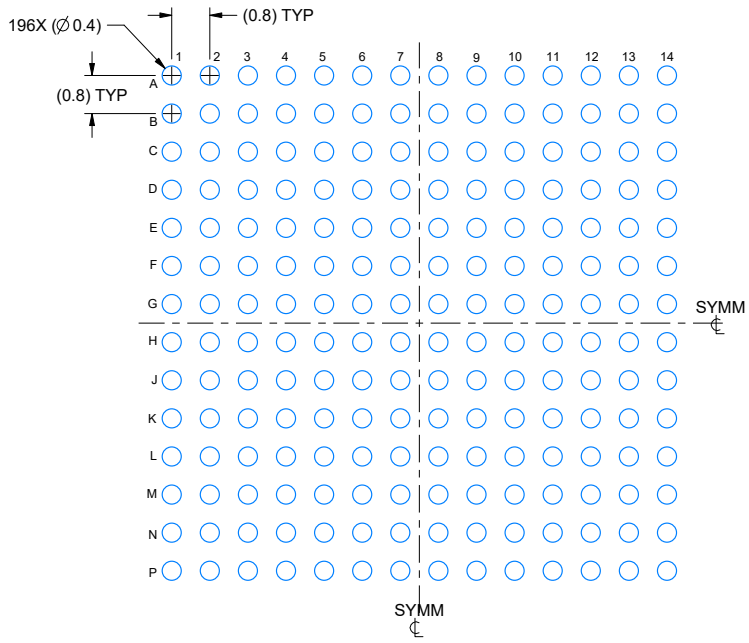
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

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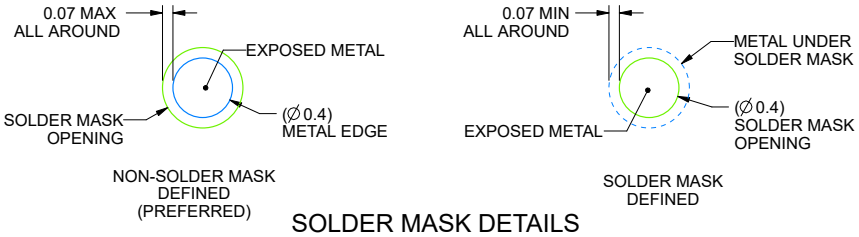
EXAMPLE BOARD LAYOUT

ACP0196A — **FCBGA - 1.321 mm max height**

BALL GRID ARRAY



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



SOLDER MASK DETAILS
NOT TO SCALE

4226793/B 07/2021

NOTES: (continued)

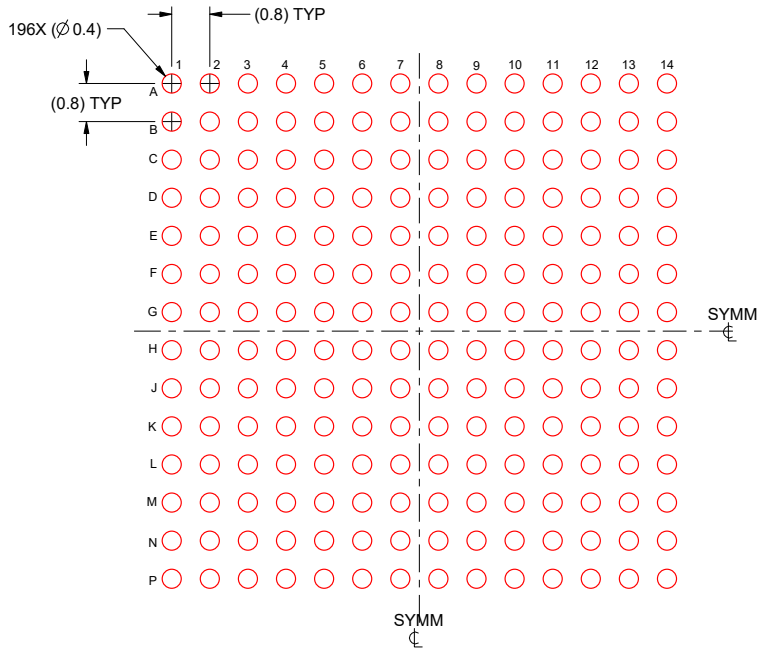
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
   For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).

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EXAMPLE STENCIL DESIGN

ACP0196A — **FCBGA - 1.321 mm max height**

BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

4226793/B 07/2021

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TX73L64ACP	Active	Production	FCCSP (ACP) | 196	160 | JEDEC TRAY (5+1)	Yes	Call TI | Snagcu	Level-3-260C-168 HR	0 to 70	TX73L64

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

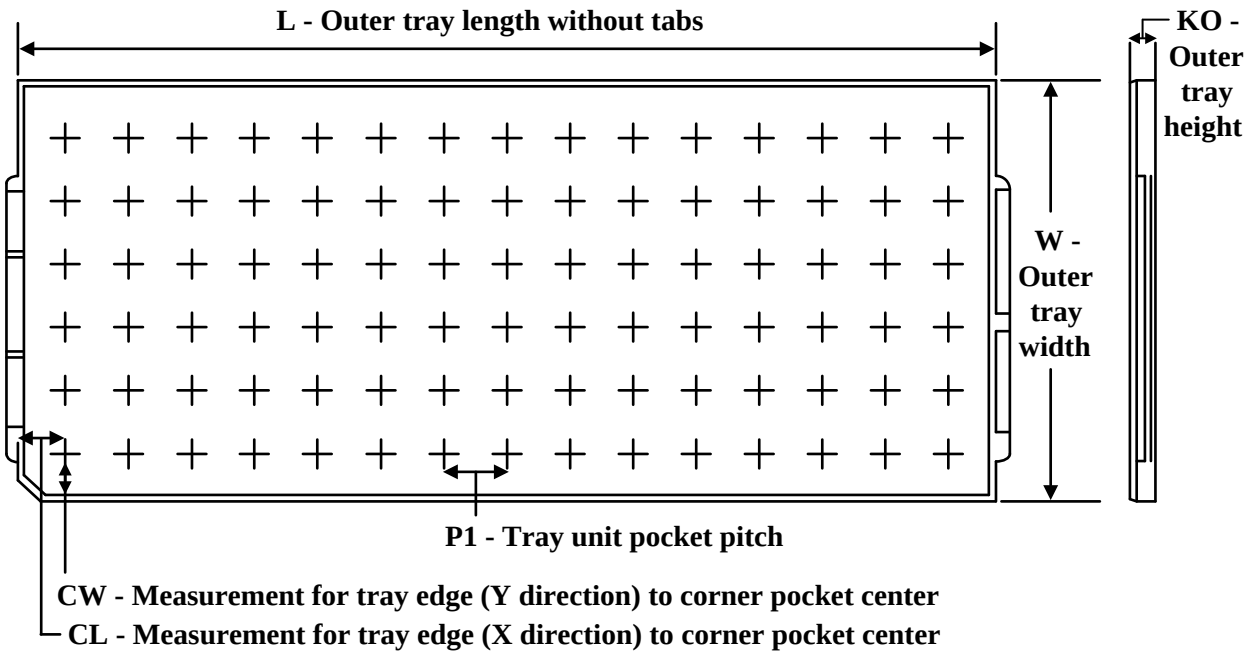
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TX73L64ACP	ACP	FCCSP	196	160	8 x 20	150	315	135.9	7620	15.4	11.2	19.65

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